REMARKS

In Election/Restrictions Response, applicant's election the invention of the Group I (claims 1-6), drawn to a device, and cancel claims 7-14 in Paper No. 3 dated on February 22, 2002, is acknowledged.

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilford (US. 6,342,723).

Response to the Office Action identified in the above is listed below.

1. Rejection over claims 1:

Regarding claim 1, Wilford discloses in Figs. 1 and 2A the bypass circuit (32, 34, 44) for reducing plasma damage to a gate oxide 22 (col.3, line 27) of a metal-oxide semiconductor (MOS) wafer, the bypass circuit positioned on a semiconductor wafer 12, the semiconductor wafer comprising a substrate 12 (col.3, line 13), the MOS transistor 14 (col.3, line 8), a dielectric layer 40 (col.3, line 65), and the bypass circuit, respectively, with the bypass circuit comprising:

a conductive wire 32 (col.3, lines 38-39) comprising at least a first contact end and a second contact end (see Fig.1), the first contact end electrically connecting with a gate electrode 26 (col.3, line 33) on the top of the MOS transistor, and the second contact end electrically connecting with a doped region P+ (col.3, line 50) in the substrate; and

a fusion area 34 (col.3, line 42) positioned in the conductive wire to disconnect the conductive wire and the MOS transistor;

wherein ions in the gate oxide are transmitted to

the doped region via the conductive wire so as to reduce plasma damage to the gate oxide (col.4, lines 8-11).

Response:

First, claim 1 is amended by merging claim 4 into claim 1 and canceling claim 4 based on the specification and figures of the present application to overcome this rejection. No new matter is introduced.

Second, the Applicants intend to point out the difference between the amended claim 1 of the present application and Wilford's disclosure. The amended claim 1 of the present application is repeated below:

1. (Once amended) A bypass circuit for reducing plasma damage to a gate oxide of a metal-oxide semiconductor (MOS) wafer, the bypass circuit positioned on a semiconductor wafer, the semiconductor wafer comprising a substrate, the MOS transistor, a dielectric layer, and the bypass circuit, respectively, with the bypass circuit comprising:

a conductive wire comprising at least a first contact end and a second contact end, the first contact end electrically connecting with a gate electrode on the top of the MOS transistor, and the second contact end electrically connecting with a doped region in the substrate; and

a fusion area positioned in the conductive wire to disconnect the conductive wire and the MOS transistor, the fusion area comprising polysilicon;

wherein ions in the gate oxide are transmitted to the doped region via the conductive wire so as to reduce

plasma damage to the gate oxide.

As disclosed in the amended claim 1 in view with the specification and figures of the present application, the fusion area is **composed of polysilicon** and is deposited in the conductive wire, **composed of tungsten**, after the conductive wire is formed. However, the sacrificial area 34 and the sacrificial conductive path 32 revealed by Wilford **have a same composition.**

In addition, the fusion area of the bypass circuit on the dielectric layer can be alternatively formed before the formation of the metal interconnect layer that electrically connects with the MOS transistor, fusion area and the n-well, as revealed in the specification of the present application. Still alternatively, the fusion area can be formed during the formation of the gate by performing the photo-etching-process used to define patterns of the gate and to form both the gate and the bypass circuit. Therefore, it is obvious that the conductive wire and the fusion area revealed in the present application are respectively different from the sacrificial conductive path 32 and the sacrificial area 34 disclosed in Wilford's invention.

From the above discussion, the Applicants believe that claim 1 of the present invention is absolutely different from Wilford's disclosure. Reconsideration of the rejection over claim 1 is hereby requested.

2. Rejection over claim 2:

Regarding claim 2, Wilford discloses in Figs.1 and 2A the bypass circuit of claim 1 wherein the conductive wire is composed of a plurality of contact plugs 42 and a metal layer 44 (col.4, lines 18-20).

Response:

As claim 2 is dependent upon claim 1, it should be allowed if claim 1 is allowed. Reconsideration of claim 2 is therefore requested.

3. Rejection over claim 3:

Regarding claim 3, Wilford discloses in Figs.1 and 2A the bypass circuit of claim 1 wherein the conductive wire is a portion of a metal interconnect layer 44 (col.4, lines 18-21).

Response:

As claim 3 is dependent upon claim 1, it should be allowed if claim 1 is allowed. Reconsideration of claim 3 is therefore requested.

4. Rejection over claim 4:

Regarding claim 4, Wilford discloses in Figs.1 and 2A the bypass circuit of claim 1 wherein the fusion area is made of polysilicon (col.3, lines 31-32).

Response:

To overcome this rejection towards claim 4, claim 4 is merged into claim 1 and is therefore cancelled.

5. Rejection over claim 5:

Regarding claim 5, Wilford discloses in Figs.1 and

2A the bypass circuit of claim 1 wherein the doped region is an n-well (col.3, lines 15-17).

Response:

As claim 5 is dependent upon claim 1, it should be allowed if claim 1 is allowed. Reconsideration of claim 5 is therefore requested.

6. Rejection over claim 6:

Regarding claim 6, Wilford discloses in Figs.1 and 2A the bypass circuit of claim 1 wherein ions in the gate oxide are transmitted to the doped region via the conductive wire so as to reduce plasma damage to the gate oxide (col.4, lines 8-11).

Response:

As claim 6 is dependent upon claim 1, it should be allowed if claim 1 is allowed. Reconsideration of claim 6 is therefore requested.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Once amended) A bypass circuit for reducing plasma damage to a gate oxide of a metal-oxide semiconductor (MOS) wafer, the bypass circuit positioned on a semiconductor wafer, the semiconductor wafer comprising a substrate, the MOS transistor, a dielectric layer, and the bypass circuit, respectively, with the bypass circuit comprising:

a conductive wire comprising at least a first contact end and a second contact end, the first contact end electrically connecting with a gate electrode on the top of the MOS transistor, and the second contact end electrically connecting with a doped region in the substrate; and

a fusion area positioned in the conductive wire to disconnect the conductive wire and the MOS transistor, the fusion area comprising polysilicon;

wherein ions in the gate oxide are transmitted to the doped region via the conductive wire so as to reduce plasma damage to the gate oxide.

Claim 4 is canceled.

Sincerely yours,

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